REMARKS

This paper is being filed as a supplement to Applicant's response filed on May 9, 2002 and is a response to the February 15, 2002 Office Action for the above-referenced application. In this supplemental response, Applicant has amended Claim12 and added new claim 18 in order to more particularly point out and distinctly claim that which Applicant deems to be the invention. Applicant respectfully submits that the modifications to the claims are all supported by the originally filed application.

Applicant thanks the Examiner for the indication of allowability with respect to dependent claims 7-8 and 13-14. In the May 9, 2002 response, Applicant has amended the claims in accordance with the suggestion in the present Office Action to rewrite claims 7 and 8 in independent form to include the features of the base claim 1. Applicant has also amended the claims to rewrite claims 13 and 14 in independent form to include the features of the base claim 2. In view of the above claims amendments Applicant respectfully requests that claims 7-8 and 13-14 be allowed.

The rejection of Claims 1-5, 9-11 and 15-17 under 35 U.S.C. §102(b) as being anticipated by Hattori (U.S. Patent No. 5,459,424 , hereinafter referred to as "Hattori") is hereby traversed and reconsideration thereof is respectfully requested. Applicants respectfully submit that Claims 1-5, 9-11 and 15-17, as amended, are patentably distinct over the cited reference.

Independent Claim 1, as amended, recites a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, having an

inverter chain containing not less than one inverter, and having a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain connected to an output section of the inverter. When a logic signal having a targeted logic level is input, it changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter. Each stage is tied alternately to one of a power voltage source and a ground voltage source. Claims 2-5 depend from independent Claim 1.

Independent Claim 2, as amended, recites a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, which has an inverter chain containing not less than one inverter, and a metal-oxide-semiconductor capacitor, known as a MOS capacitor, comprising a single transistor per stage of the inverter chain connected to an output section of the inverter and exhibiting changes in its capacitance to correspond with changes in output resistance of the inverter in relation to a source voltage. Each stage is tied alternately to one of a power voltage source and a ground voltage source. Claims 9-11 depend from independent Claim 2.

Independent Claim 15, as amended, recites a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, which has an inverter chain containing not less than one inverter, and a p-channel metal-oxide-semiconductor transistor and an n-channel metal-oxide-semiconductor transistor, known as MOS transistors, to comprise the inverter, wherein a gate threshold voltage of each gate is shifted in mutually opposing directions.

Independent Claim 16, as amended, recites a method for delaying a logic signal having two logic levels consisting of a low level and a high level, having the steps of setting a metal-oxide-semiconductor capacitor disposed on a transmission path of a logic signal to an off-state in an initial stage, and changing the metal-oxide-semiconductor capacitor to an on-state from the off-state according to a logic level of the logic signal. Claim 17 depends from claim 16.

The cited art of Hattori discloses a CMOS pulse delay circuit that can accurately delay a signal by a predetermined amount. There are disclosed inverters that each have additional switching transistors on each end, and a voltage controlled variable resistor. The indicated portion of the reference discloses a CMOS inverter that has both an N channel and a P channel transistor located after each stage of the inverter chain.

Applicant respectfully submits that the cited reference does not contain the recited feature of a delay circuit "... *comprising a single transistor per stage of the inverter chain* ...", as set forth in Applicant's independent claim 1, as amended. Rather, the cited reference of Hattori has two transistors per stage of the inverter chain, with one tied to power and one tied to ground. Therefore, since the cited reference does not contain each and every feature of the claimed invention, the cited reference can not anticipate independent Claim 1.

Applicant further respectfully submits that the cited reference does not contain the recited feature of a delay circuit "... *comprising a single transistor per stage of the inverter chain* ...", as set forth in Applicant's independent claim 2, as amended. Rather, the cited reference of Hattori has two transistors per stage of the inverter chain, with one tied to power and one tied to ground. Therefore, since the cited reference does not contain each and every feature of the claimed invention, the cited reference can not anticipate independent Claim 2.

Applicant further respectfully submits that the cited reference does not contain the recited feature of a delay circuit "... *to comprise the inverter, wherein a gate threshold voltage of each gate is shifted in mutually opposing directions* ...", as set forth in Applicant's independent claim 15. Rather, the cited reference of Hattori has the two transistors per stage of the inverter chain, each having matched absolute values of threshold, as is standard practice in CMOS integrated circuit designs. Claim 15 is illustrated in figure 8 of the present application, and discussed on page 29, which shows that the present claimed arrangement has the PMOS of the first inverter stage set for a higher than normal absolute value of threshold voltage, while the NMOS of the first inverter stage has a lower than normal absolute threshold. The opposite is true of the second inverter stage. There is no disclosure of any type related to this sort of arrangement in the cited reference of Hattori. Therefore, since the cited reference does not contain each and every feature of the claimed invention, the cited reference can not anticipate independent Claim 15.

Applicant further respectfully submits that the cited reference does not contain the recited feature of a delay circuit "... *setting a metal-oxide-semiconductor capacitor disposed on a transmission path of a logic signal to an off-state in an initial stage* ...", as set forth in Applicant's independent claim 16. There is no disclosure of any type related to this sort of arrangement in the cited reference of Hattori. Therefore, since the cited reference does not contain each and every feature of the claimed invention, the cited reference can not anticipate independent Claim 16.

For at least the above discussed reasons, Applicant respectfully submits that the independent Claims, as amended, and thus the dependent Claims, are patentably distinct over the cited reference, and respectfully requests that this rejection be withdrawn.

The rejection of Claims 1-4, 9-10 and 16-17 under 35 U.S.C. §102(b) as being anticipated by Usuki et al (U.S. Patent No. 5, , hereinafter referred to as "") is hereby traversed and reconsideration thereof is respectfully requested. Applicants respectfully submit that Claims 1-4, 9-10 and 16-17, as amended herein, are patentably distinct over the cited reference.

The independent claims are discussed above.

The cited art of Usuki discloses a delay circuit for integrated circuits that has a pair of MIS transistors with a constant current source and a capacitance. The indicated portion of the reference discloses a series of inverters, each with a capacitance to ground.

Applicant respectfully submits that the cited reference does not contain the recited feature of "... *a metal-oxide-semiconductor capacitor, known as a MOS capacitor, comprising a single transistor per stage of the inverter chain connected to an output section of the inverter and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter* ...", as set forth in Applicant's independent claim 1, as amended. Rather, the cited reference at the indicated location does not have any active device that can change from an off state to an on state depending upon the output of the particular inverter stage. Therefore, since the cited reference does not contain each and every feature of the claimed invention, the cited reference can not anticipate independent Claim 1. Similar arguments may be easily made for the features of each of the other independent claims in the present application.

For at least the above discussed reasons, Applicant respectfully submits that independent Claims 1, 2 and 16, as amended, and thus the dependent Claims which depends therefrom, are patentably distinct over the cited reference, and respectfully requests that this rejection be withdrawn.

The rejection of Claims 1-6, 9-12 and 16-17 under 35 U.S.C. §102(e) as being anticipated by Porter et al (U.S. Patent No. 6,040,713, hereinafter referred to as "Porter") is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that Claims 1-6, 9-12 and 16-17, as amended, are patentably distinct over the cited reference, for the reasons set forth below.

The features of the present claims are discussed above.

The cited art of Porter discloses a buffers with fast edge propagation having at least two input terminals and one output terminal. The input signal terminal being connected to a first buffer terminal, and a shielding circuit connected to the other input terminal. There is a recovery circuit connected to the shielding circuit connected to the second input terminal of the buffer. The indicated portion of the reference discloses a delay line having a series of inverters, each having an NMOS transistor having its gate tied to the inter inverter node, and the source and drain tied to ground.

Applicant respectfully submits that the cited reference does not contain the recited feature of "... *each stage is tied alternately to one of a power voltage source and a ground voltage source* ....", as set forth in independent Claim 1. Rather, the cited reference of Porter, as noted above, has each stage connected to ground, as opposed to the claimed arrangement of alternating power with ground connections. Therefore, since the cited reference does not contain each and every feature of the claimed invention, the cited reference can not anticipate independent Claim 1.

Applicant respectfully submits that the cited reference does not contain the recited feature of "... *each stage is tied alternately to one of a power voltage source and a ground voltage source* ....", as set forth in independent Claim 2. Rather, the cited reference of Porter, as noted above, has each stage connected to ground, as opposed to the claimed arrangement of alternating power with ground connections. Therefore, since the

cited reference does not contain each and every feature of the claimed invention, the cited reference can not anticipate independent Claim 2.

Applicant respectfully submits that the cited reference does not contain the recited feature of "..."... *setting a metal-oxide-semiconductor capacitor disposed on a transmission path of a logic signal to an off-state in an initial stage* ...", as set forth in Applicant's independent claim 16. There is no disclosure of any type related to this sort of arrangement in the cited reference of Porter. Therefore, since the cited reference does not contain each and every feature of the claimed invention, the cited reference can not anticipate independent Claim 16.

Accordingly, Applicant respectfully submits that the independent claims, and thus the claims which depends therefrom, are patentably distinct over the cited reference, and respectfully requests that this rejection be withdrawn.

With respect to new independent claim 18, Applicant notes that lines 5 to 8 on page 4 of the specification, indicate that an object of the present invention is to provide a delay circuit having a low dependency on the power source voltage (that is, do not lead to excessive increase in the delay time even if the source voltage drops, so as to enable to control the delay time from increasing).

According to the recitation of claim 18, a delay circuit having a low dependence on the power source voltage for either the rising edge or the falling edge of the input

signal can be provided. In claim 18, when the logic signal having the logic level targeted for delay is input into the head gate circuit, all MOS capacitors are connected so as to turn from the off-state to the on-state. The capacity between the gate and the drain and source of the MOS capacitors becomes small because a depletion layer forms directly below the gates when the MOS capacitors are in the off-state. When the MOS capacitors are in the on-state, an inversion layer formed directly under the gate connects to the source and drain, and thus the capacity becomes large. Further note that the delay time for each inverter state is determined by the time from the change of the output signal of the inverter until the MOS capacitors charge and the level of the output signal attains the threshold level of the inverter of the next stage. At this time, the MOS capacitor changes from an off-state (low capacity) to the on-state (high capacity). Here, rather than when the power source voltage is high, when it is low, the low capacity of the off-state is controlling, and as a result, the dependency on the power source voltage described above becomes small.

Thus, in claim 18, when a logic signal having the logic level targeted for delay is input, all of the MOS capacitors are connected so as to turn from the off-state to the on-state. In contrast, in Fig. 1 of Hattori, when the input signal I arrives at a high level, the MOS capacitor 27 changes from an off-state to an on-state, and the MOS capacitor 28 changes from the on-state to the off-state. In addition, in Fig. 5 of Usuki and Fig. 11 of Porter, in the case, for example, that the capacitors in the even-numbered stages change from the off-state to the on-state, the capacitors in the odd-numbered stages change from

the on-state to the off-state. In this manner, in each of the above citations, it is not the case that all of the MOS capacitors together change from the off-state to the on-state.

Accordingly, claim 18 is patentable over each of the cited references alone or in any combination.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-951-6676.

Respectfully submitted,
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